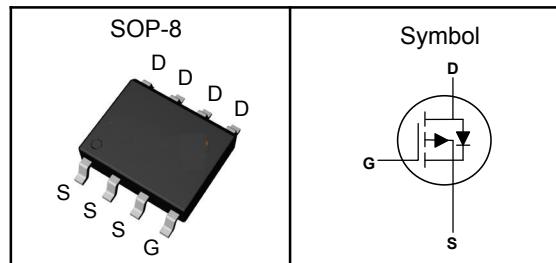


P-Channel Enhancement Mode MOSFET

Features

- Advanced Trench technology
- High Speed Power Switching
- Reliable and Rugged
- ROHS Compliant
- 100% Avalanche Tested

Pin Description



Applications

- Power Management in Desktop Computer
- DC/DC Converters

V_{DSS}	-60	V
$R_{DS(ON)-Typ}$	75	$\text{m}\Omega$
I_D	-10	A

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-60	V
V_{GSS}	Gate-Source Voltage	± 20	V
T_J	Maximum Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$I_{DM}^{①}$	Pulse Drain Current Tested	-45	A
I_D	Continuous Drain Current	$T_c=25^\circ\text{C}$	-10
I_D	Continuous Drain Current	$T_c=100^\circ\text{C}$	-4
P_D	Maximum Power Dissipation	35	W

Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	---	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	4	$^\circ\text{C}/\text{W}$

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150°C .

Note ③ : Surface Mounted on 1in² FR-4 board with 1oz.

P-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^\circ\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static Electrical Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=-250\mu\text{A}$	-60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-60\text{V}$, $V_{\text{GS}}=0\text{V}$	---	---	-1	μA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=-250\mu\text{A}$	-1.2	---	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
$R_{\text{DS}(\text{ON})}$	Drain-Source On-state Resistance	$V_{\text{GS}}=-10\text{V}$, $I_D=-6\text{A}$	---	75	90	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}$, $I_D=-10\text{A}$	---	90	115	$\text{m}\Omega$
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	15	---	Ω
Dynamic Characteristics^⑤						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=-30\text{V}$, Freq.=1MHz	---	1021	---	pF
C_{oss}	Output Capacitance		---	64	---	
C_{rss}	Reverse Transfer Capacitance		---	53	---	
$T_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DD}}=-30\text{V}$, $V_{\text{GS}}=-10\text{V}$, $R_G=3.3\Omega$, $I_D=-1\text{A}$	---	8.8	---	nS
T_r	Turn-on Rise Time		---	12	---	
$T_{\text{d}(\text{off})}$	Turn-off Delay Time		---	25	---	
T_f	Turn-off Fall Time		---	18	---	
Q_g	Total Gate Charge	$V_{\text{DS}}=-30\text{V}$, $V_{\text{GS}}=-10\text{V}$, $I_D=-10\text{A}$	---	16	---	nC
Q_{gs}	Gate-Source Charge		---	1.9	---	
Q_{gd}	Gate-Drain Charge		---	5	---	
Source-Drain Characteristics ($T_J=25^\circ\text{C}$)						
$V_{\text{SD}}^{④}$	Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_S=-2\text{A}$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

Note ④ : Pulse test (pulse width≤300us, duty cycle≤2%).

Note ⑤ : Guaranteed by design, not subject to production testing.

P-Channel Enhancement Mode MOSFET

Typical Characteristics

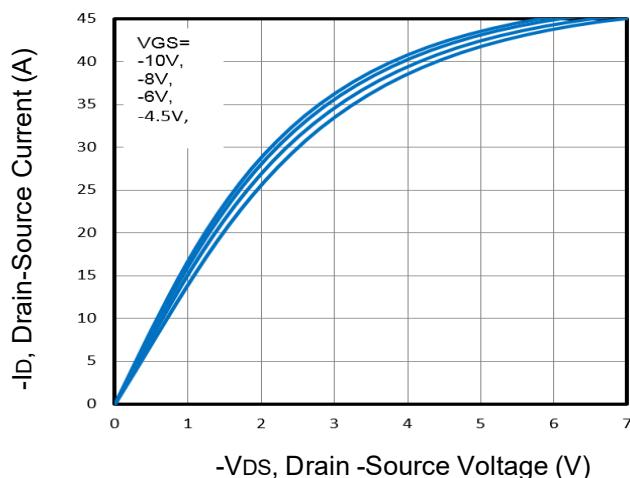


Fig1. Typical Output Characteristics

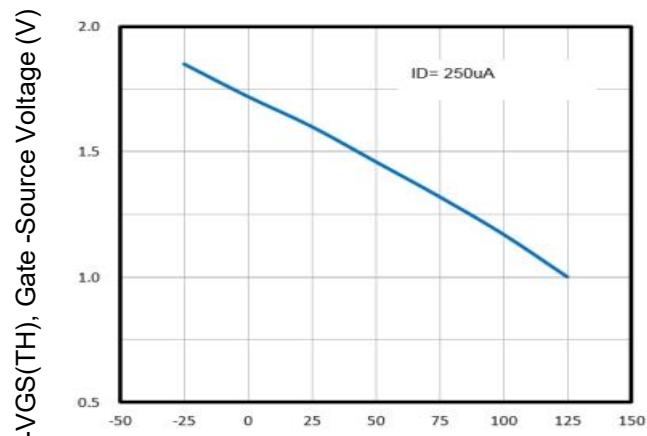


Fig2. Normalized Threshold Voltage Vs. Temperature

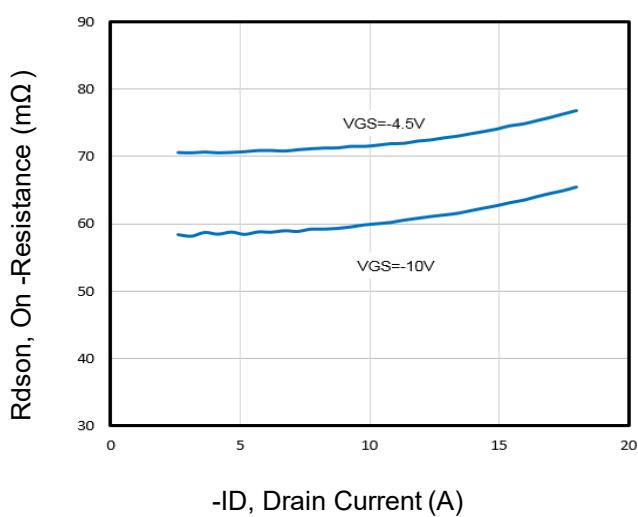


Fig3. On-Resistance vs. Drain Current and Gate

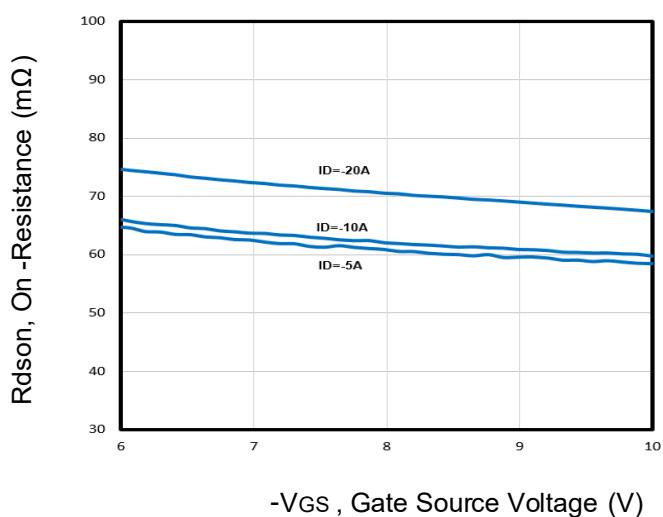


Fig4. On-Resistance vs. Gate Source Voltage

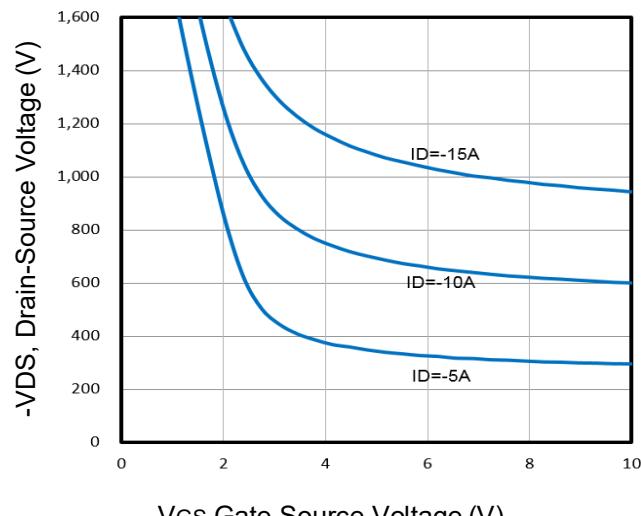


Fig5. Drain-Source Voltage vs Gate-Source Voltage

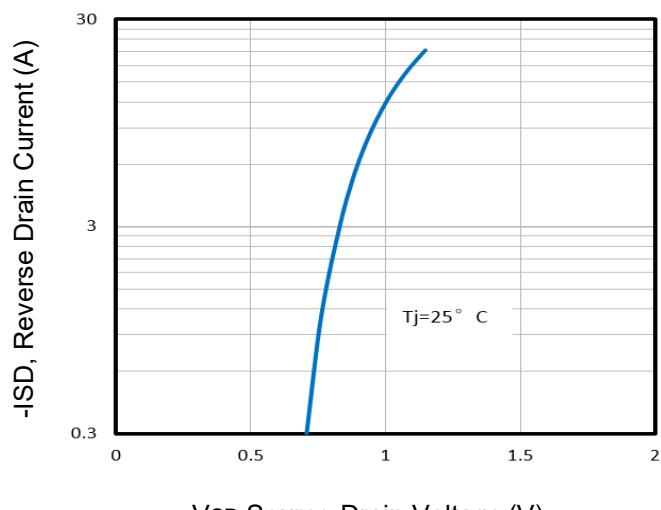


Fig6. Typical Source-Drain Diode Forward Voltage

P-Channel Enhancement Mode MOSFET

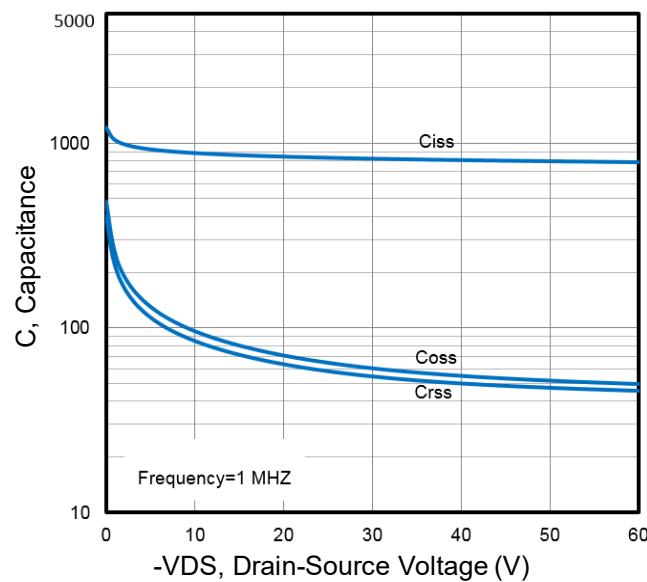


Fig7. Typical Capacitance Vs. Drain-Source Voltage

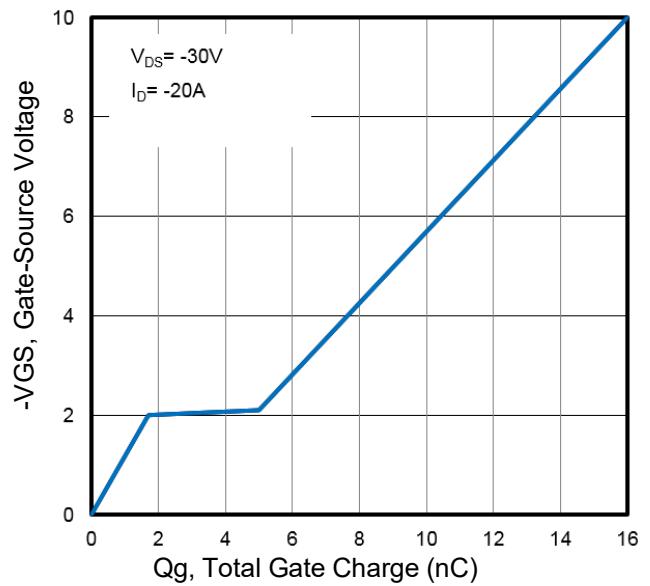
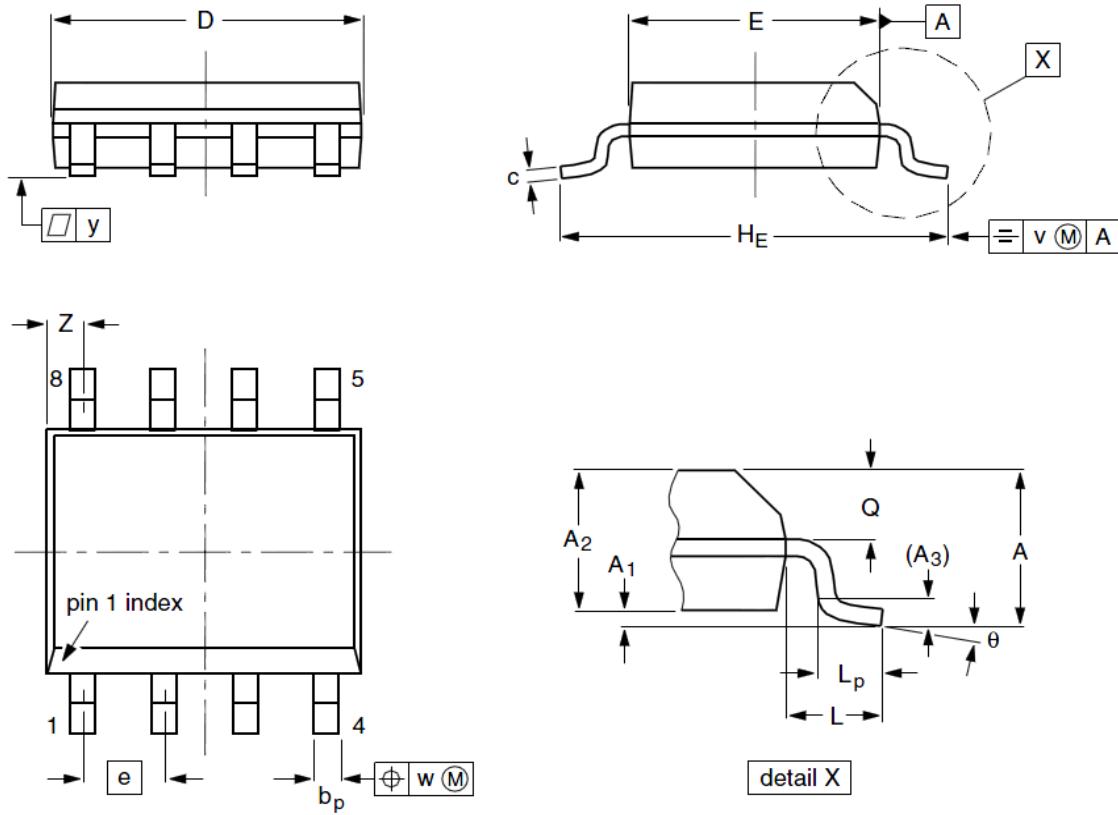


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

P-Channel Enhancement Mode MOSFET

SOP-8 Package Outline Dimensions



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	1.35	1.55	1.75	A₁	0.10	0.18	0.25
A₂	1.25	1.45	1.65	A₃	--	0.25	--
b_p	0.36	0.42	0.51	c	0.19	0.22	0.25
D	4.70	4.92	5.10	E	3.80	3.90	4.00
e	--	1.27	--	H_E	5.80	6.00	6.20
L	--	1.05	--	L_P	0.40	0.68	1.00
Q	0.60	0.65	0.73	v	--	0.25	--
w	--	0.25	--	y	--	0.10	--
Z	0.30	0.50	0.70	θ	0°		8°



FSL06P75JS

P-Channel Enhancement Mode MOSFET

印字说明

印字说明

FSL06P75JS

AABBCC

第一行标记为物料型号代码

第二行为AA为内部识别码，BB为表示年份，例如22即表示2022年，CC表示周期，例如01即表示第一周；
2201即表示2022年第一周生产。