

## P-Channel Enhancement Mode MOSFET

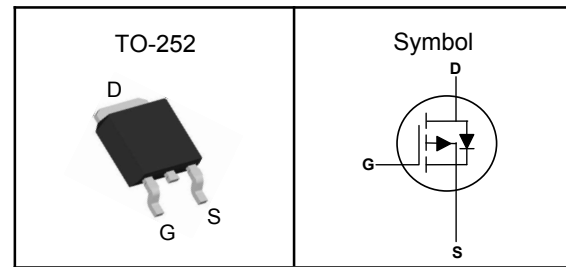
### Features

- Advanced trench cell design
- Low Thermal Resistance
- ROHS Compliant & Halogen-Free
- 100% UIS and Rg Tested

### Applications

- Motor drivers
- DC - DC Converter

### Pin Description



$V_{DSS}$	-40	V
$R_{DS(ON)-Typ}$	5.0	m $\Omega$
$I_D$	-90	A

### Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit
$V_{DSS}$	Drain-Source Voltage	-40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$T_J$	Maximum Junction Temperature	-55 to 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
$I_{DM}^{①}$	Pulse Drain Current Tested	-339	A
$I_D$	Continuous Drain Current	-90	A
$P_D$	Maximum Power Dissipation	58	W

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.3	$^\circ\text{C/W}$

Note ① : Max. current is limited by bonding wire.

Note ② : UIS tested and pulse width are limited by maximum junction temperature 150 $^\circ\text{C}$ .

Note ③ : Surface Mounted on 1in<sup>2</sup> FR-4 board with 1oz.

**P-Channel Enhancement Mode MOSFET****Electrical Characteristics** ( $T_J=25^\circ\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Static Electrical Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	---	---	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-40V, V_{GS}=0V$	---	---	-1	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	---	-2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$R_{DS(on)}$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_D=-20A$	---	5.0	6.0	m $\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	---	6.5	8.0	m $\Omega$
<b>Dynamic Characteristics<sup>⑤</sup></b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0V, V_{DS}=-20V, \text{Freq.}=1\text{MHz}$	---	5545	---	pF
$C_{oss}$	Output Capacitance		---	454	---	
$C_{rss}$	Reverse Transfer Capacitance		---	287	---	
$T_{d(on)}$	Turn-on Delay Time	$V_{GS}=-10V, V_{DD}=-20V, I_D=-1A, R_G=1.6\Omega$	---	16	---	nS
$T_r$	Turn-on Rise Time		---	17	---	
$T_{d(off)}$	Turn-off Delay Time		---	68	---	
$T_f$	Turn-off Fall Time		---	31	---	
$Q_g$	Total Gate Charge	$V_{GS}=-10V, V_{DD}=-20V, I_D=-8A$	---	127	---	nC
$Q_{gs}$	Gate-Source Charge		---	13	---	
$Q_{gd}$	Gate-Drain Charge		---	22	---	
<b>Source-Drain Characteristics</b>						
$V_{SD}^{④}$	Diode Forward Voltage	$I_S=-8A, V_{GS}=0V$	---	---	-1.2	V

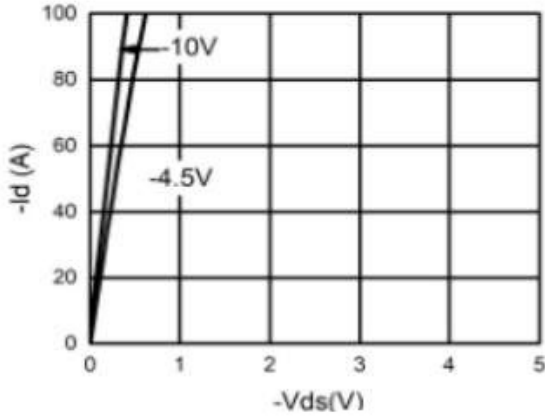
Note ④: Pulse test (pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ ).

Note ⑤: Guaranteed by design, not subject to production testing.

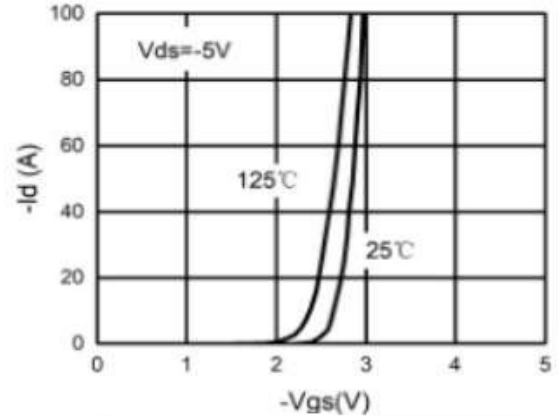
**P-Channel Enhancement Mode MOSFET**

**Typical Characteristics**

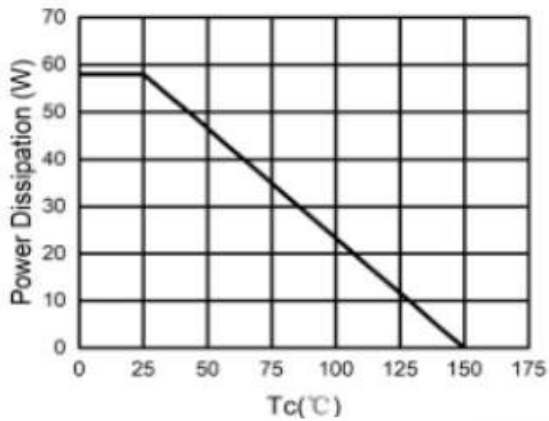
**Figure 1. Output Characteristics**



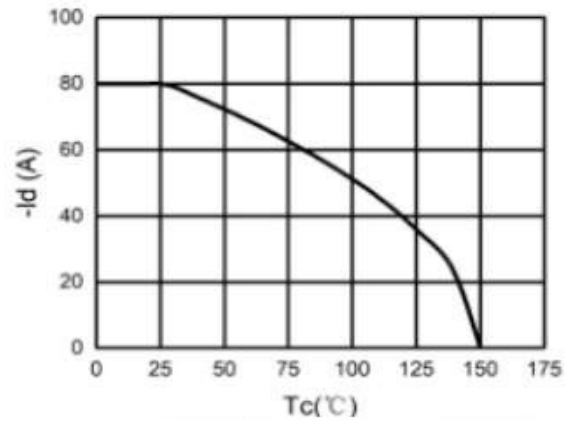
**Figure 2. Transfer Characteristics**



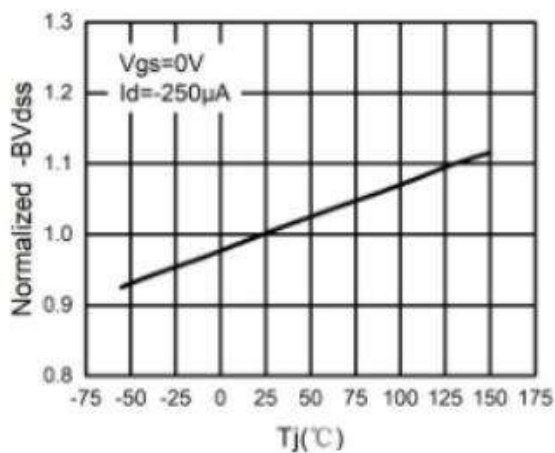
**Figure 3. Power Dissipation**



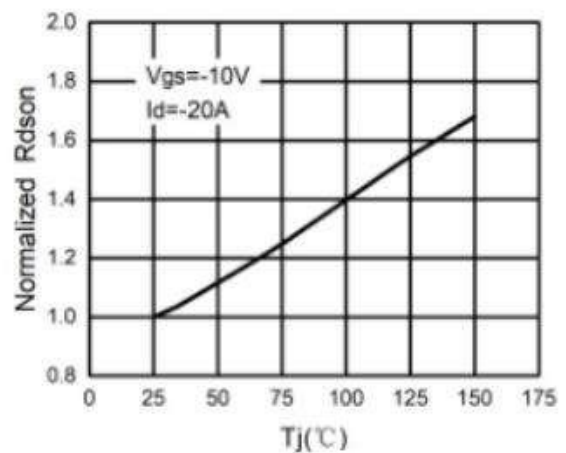
**Figure 4. Drain Current**



**Figure 5.  $BV_{DSS}$  vs Junction Temperature**

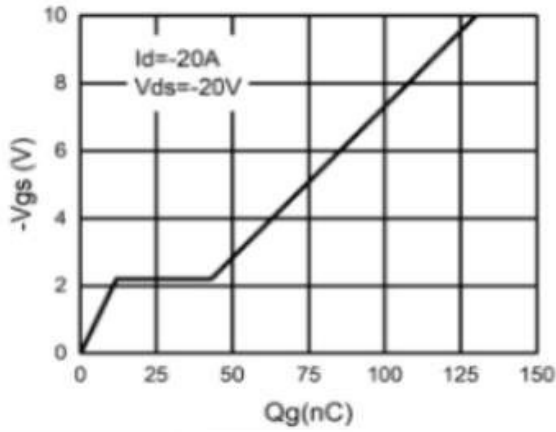


**Figure 6.  $R_{DS(ON)}$  vs Junction Temperature**

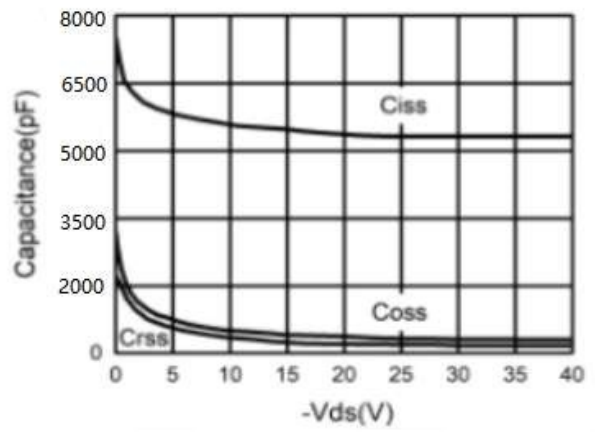


**P-Channel Enhancement Mode MOSFET**

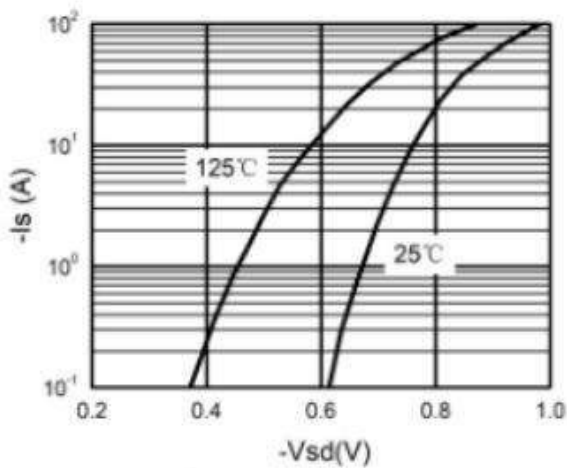
**Figure 7. Gate Charge Waveforms**



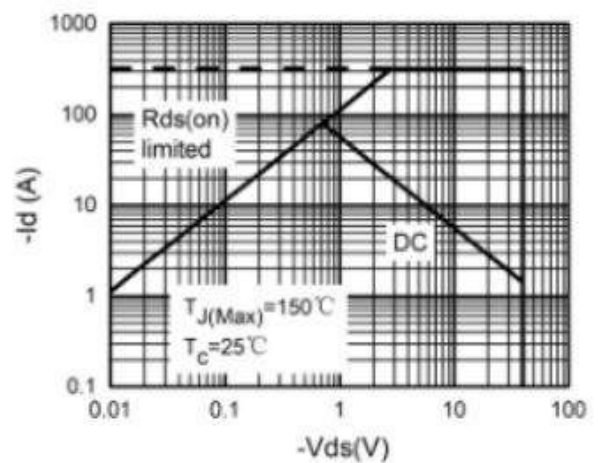
**Figure 8. Capacitance**

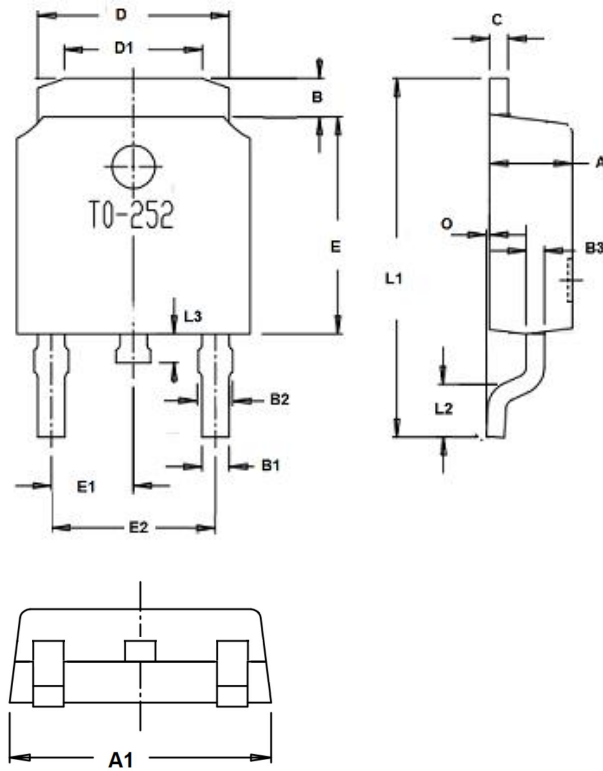


**Figure 9. Body-Diode Characteristics**



**Figure 10. Maximum Safe Operating Area**



**P-Channel Enhancement Mode MOSFET**
**TO-252 Package Outline Dimensions**


Dim.	Min.	Max.
A	2.1	2.5
A1	6.3	6.9
B	0.96	1.42
B1	0.74	0.86
B2	0.74	0.94
C	Typ0.5	
D	5.33	5.53
D1	3.65	4.05
E	6.0	6.2
E1	Typ2.29	
E2	Typ4.58	
O	0	0.15
L1	9.9	10.5
L2	Typ1.65	
L3	0.6	1.0
All Dimensions in millimeter		



## 印字说明

### 印字说明

FSL04P05AD

AABBCC

第一行标记为物料型号代码

第二行为AA为内部识别码，BB为表示年份，例如22即表示2022年，CC表示周期，例如01即表示第一周；2201即表示2022年第一周生产。